Enhancement of Back Gate Bias to Reduce Power Dissipation in Domino Inverter by Lower Adaptive Voltage Level Circuit

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Abstract – Lower Adaptive voltage level circuit – with its negative clk, can supply more dc voltage to inverter in active mode & with positive clk Vss in standby mode is developed. This circuit can enhance back gate bias to reduce the leakage power in electronics. The leakage power dissipation in static cmos Inverter is 23% high than lower adaptive voltage level domino inverter circuit. This circuit is implemented in DSCH & Microwind. Moreover power consumption of low adaptive voltage level circuit of Domino inverter is 23 % less than conventional cmos Inverter.

Index Terms – Lower Adaptive Voltage Level circuit (LAVL), Subthreshold leakage, Domino Inverter, Static CMOS inverter.

1. INTRODUCTION

Dynamic circuits such as domino logic circuits are widely used in high performance microprocessors for obtaining high speeds that are not possible with static CMOS circuits .Their high speed is due to reduced input capacitance, small switching thresholds and circuit implementations that typically use fewer levels of logic due to the usage of efficient and wide complex logic gates. But the penalty to be paid for speed improvement is the increased power dissipation, mainly due to the necessary clocking and increased noise sensitivity. Hence, this imposes the challenges in the design of dynamic circuits. Further, as the technology is continuously scaled, reduction in power supply voltage is necessary to reduce the dynamic power and avoid reliability problems in deep submicron (DSM) regimes. This supply voltage scaling necessitates a corresponding reduction in threshold voltage in order to maintain performance, which in turn causes an exponential increase in subthreshold leakage currents and they become a major contributor to the total power dissipation. Also, the noise margin gets reduced thereby making the circuits more sensitive to noise. This provides the motivation to explore various techniques that can be applied to reduce leakage power in domino logic circuits. The leakage current of a transistor is mainly the result of reverse biased PN junction leakage and Sub threshold leakage. Compared to the subthreshold leakage, the reverse bias PN junction leakage can be ignored. The Subthreshold conduction or the subthreshold leakage or the subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage due to decreased transistor currents. One of the technique is to employ a voltage control circuit to reduce leakage.

2. RELATED WORK

2.1. STATIC CMOS INVERTER

In the Inverter circuit when clkdata is low, Pmos conducts, Nmos is in off state & output voltage is Vdd.,When clkdata is high Nmos conducts ,Pmos is in off state so output is low. Inverter is implemented in 90 nm technology using Microwind. The schematic diagram & power dissipation is shown in fig 1,6 & 7. Vdd Supply of 1.2 volt is given ,input sequence of 01010 is given.

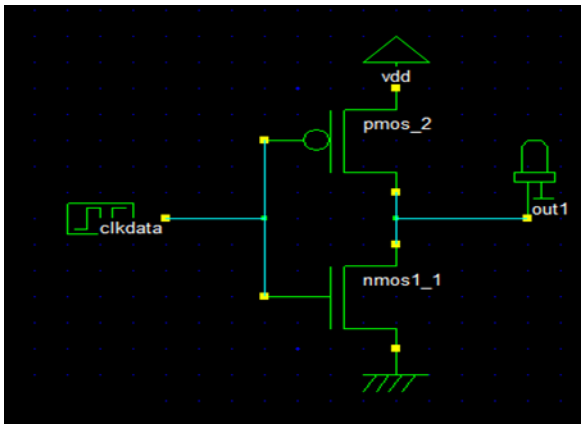

Figure1. Static Cmos Inverter

2.2. DOMINO INVERTER

Domino style incorporates clk inputs to all gates.The operation of these gates is divided into 2 phases. The phases are precharge & evaluation . In the precharge phase gate outputs are charged to high level voltage because PMOS transistors are controlled by clock input which in this phase is low .In the evaluate phase, the outputs of the gate can conditionally change to low voltage level. The logic of the gate is implemented only with NMOS transistors those transistors dictate if the outputs will be connected to the low voltage level to be discharged or

not.. Domino Inverter is implemented in 90 nm technology using Microwind. When clkdata is low ,in precharge state Pmos1 conducts output is driven depending on clk data i.e pmos2 conducts so output is charged to Vdd, in evaluate phase clk1 is high so nmos2 conducts & nmos1 doesn't conduct so out1 retains the charge. When clkdata is high nmos1 conducts ,in precharge phase pmos1 conducts, so output is reduced as it discharges since pmos2 is off & in evaluate phase nmos2 conducts so output is pulled down to 0.The schematic diagram & voltage, current curve is shown in fig 2 & 7.Vdd Supply of 1.2 volt is given, input sequence is 01010.

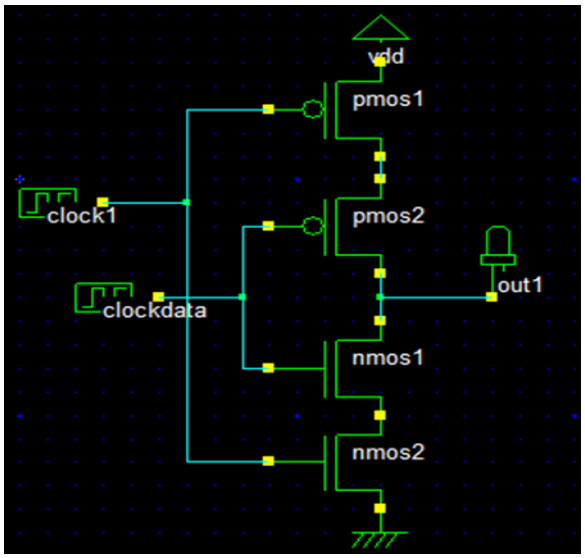

Figure 2.Domino Inverter

3. PROPOSED WORK

3.1. ADAPTIVE VOLTAGE LEVEL CIRCUIT (AVL)

Reduction in threshold voltage results in the increase in sub-threshold leakage current. One of the challenge with technology scaling is the rapid increase in subthreshold leakage power due to Vt reduction. In such a system it becomes crucial to identify techniques to reduce this leakage power component. Leakage power control can be divided into two categories - Leakage Control in Standby Mode of load, Leakage Control in Active Mode of load. In the active mode of load the 2PMOS in LAVL circuit is turned on so that a drop of v occurs in each Pmos & Vs is supplied to load circuit which increases the depletion region between source & substrate .

Vs=Vss+2v (active mode)

Vs=Vss (standby mode)

Vs=node voltage between load & LAVL circuit

Vss=Source to source voltage

v=Voltage drop in each PMOS

Furthermore source voltage (*Vs*) is increased by *mv*, so the substrate bias (i.e., back-gate bias) (*V*sub) expressed by

Vsub = – mv,

is increased .The increase in the back-gate bias (BGB) effect lead to increase in *V*thn. This results in a decrease in the subthreshold current of the n-MOS (Istn); that is, the leakage current through the inverter decreases & power dissipation also decreases.

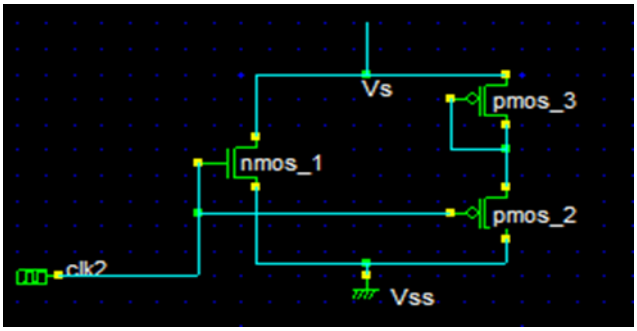

Figure 3. Adaptive Voltage Level Circuit

3.2. LOWER ADAPTIVE VOLTAGE LEVEL CIRCUIT WITH STATIC CMOS INVERTER AS LOAD

In Lower Adaptive Voltage Level Circuit with Static CMOS Inverter as load when low clk2 is applied to control circuit 2 Pmos gets on & supplies 2v to load if Nmos of load is in active mode else in standby mode & in high clk2 condition Nmos of control circuit is on & supplies Vss to Nmos in load .This is implemented in 90 nm technology using Microwind.

The schematic diagram & power dissipation & currents is shown in fig 4 ,10 &11.Vdd Supply of 1.2 volt is given, input sequence is 01010.

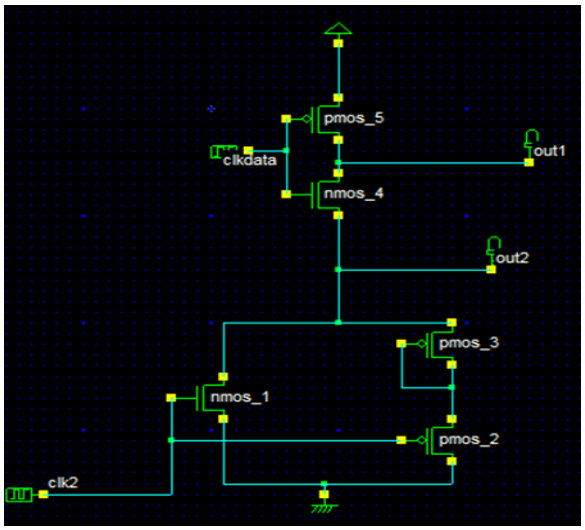

Figure 4 .Lower Adaptive Voltage Level Circuit with Static CMOS Inverter as load

3.3. LOWER ADAPTIVE VOLTAGE LEVEL CIRCUIT WITH DOMINO INVERTER AS LOAD

Lower Adaptive Voltage Level Circuit with domino Inverter as load is implemented in 90 nm technology using Microwind.The schematic diagram & leakage curve is shown in fig 5 & 9.Vdd Supply of 1.2 volt is given, input sequence is 01010.

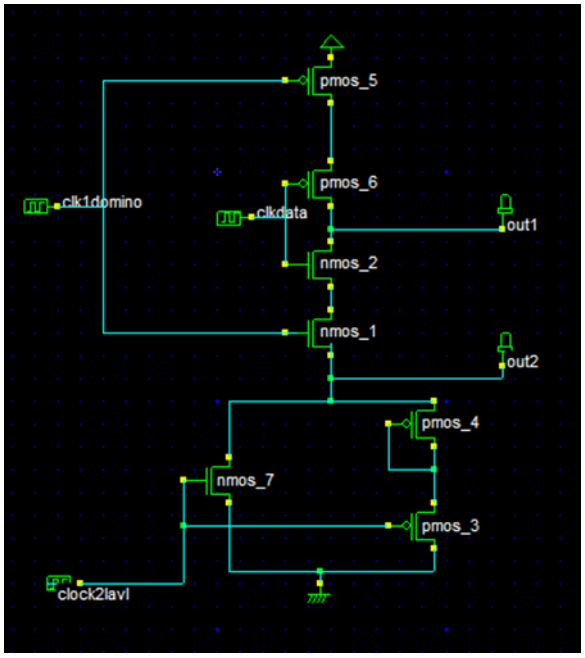

Figure 5. Lower Adaptive Voltage Level Circuit with Domino Inverter as load

4. RESULTS & DISCUSSION

4.1 Static Cmos Inverter

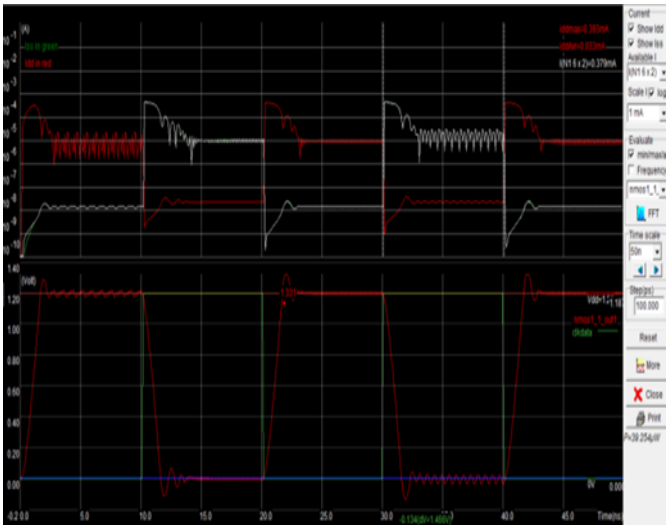

Figure 6.Voltage Current waveforms for Static Cmos Inverter

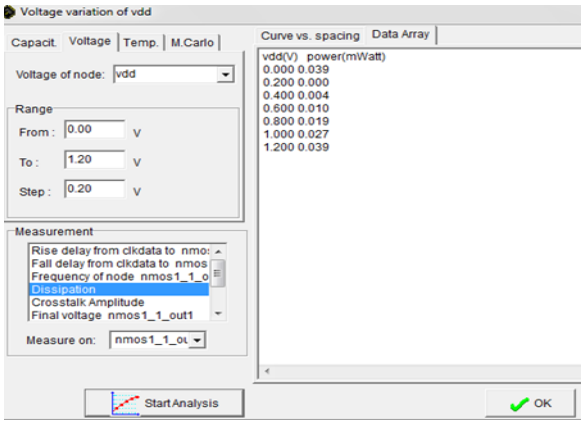

Figure 7.Leakage power dissipation for Static Cmos Inverter

Power consumption is 39.254µW which is 23% more than Adaptive Voltage Level Circuit with Domino Inverter as load.The average drain current is 0.033 mW. which is 24% greater than Adaptive Voltage Level Circuit with Domino Inverter as load Propagation delay is 900 ps.Power dissipation is 0.039mW

4.2 Domino Inverter

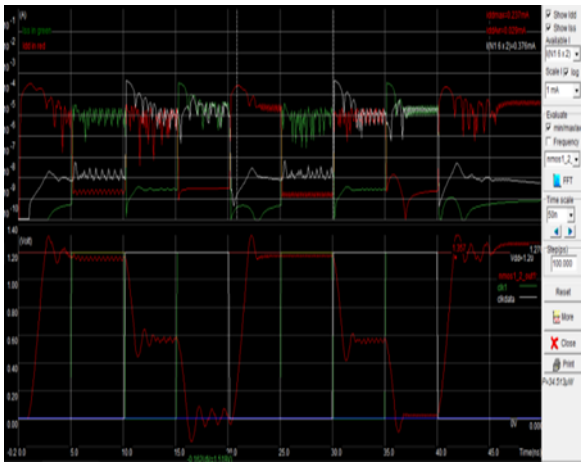

Figure 8. Voltage Current waveforms for Domino Inverter

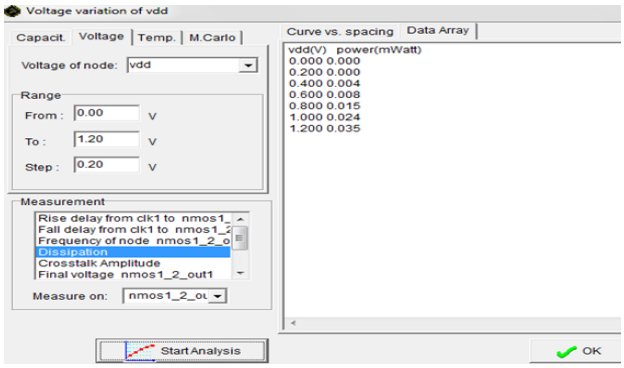

Figure 9.Leakage power dissipation for Domino Inverter

Power consumption is 34.513µW .The average drain current is 0.029 mW.. Propagation delay is 1050ps.Power dissipation is 0.035mW.

4.3 Lower Adaptive Voltage Level Circuit with Static CMOS Inverter as load

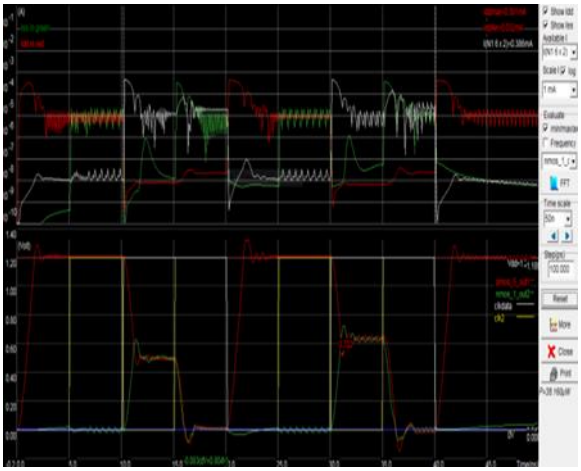

Figure 10 . Voltage Current waveforms for Lower Adaptive Voltage Level Circuit with Static CMOS Inverter as load

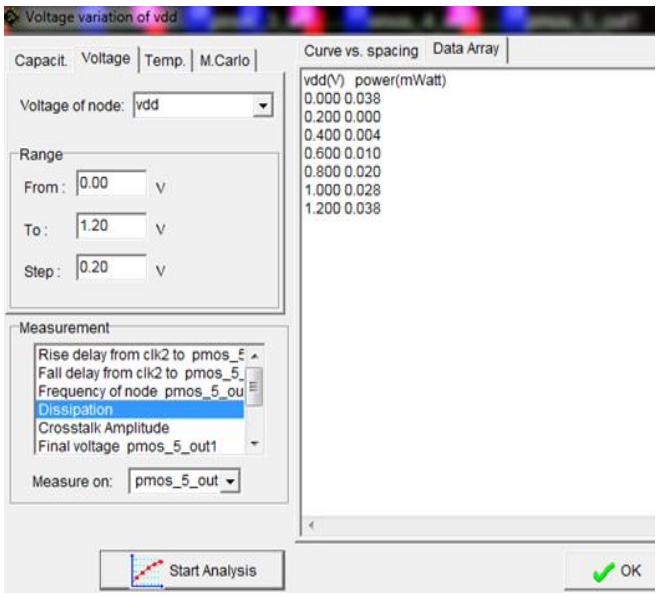

Figure 11 . Leakage power dissipation for Lower Adaptive Voltage Level Circuit with Static CMOS Inverter as load

Power consumption is 38.160µW.The average drain current is 0.032 mW. Propagation delay is 1000 ps. Power dissipation is 0.038mW.Voltage at node between load & control circuit is shifted to 0.722 from 0 i.e voltage of source increases so depletion region at source bulk increases , this increases the threshold voltage & hence reduction in leakage current. currents Idd & Iss is shown in simulation output.

4.4 Lower Adaptive Voltage Level Circuit with Domino Inverter as Load

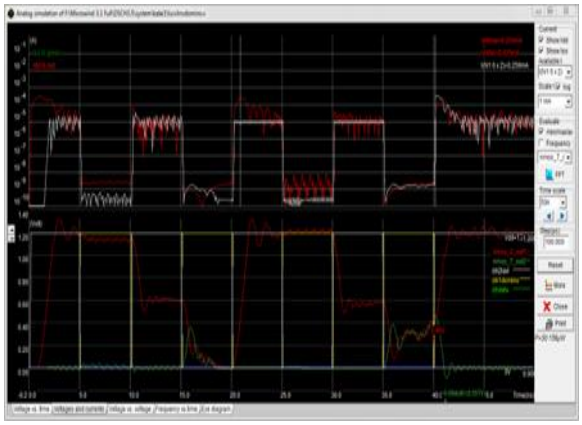

Figure 12. Voltage Current waveforms for Lower Adaptive Voltage Level Circuit with Domino Inverter as Load

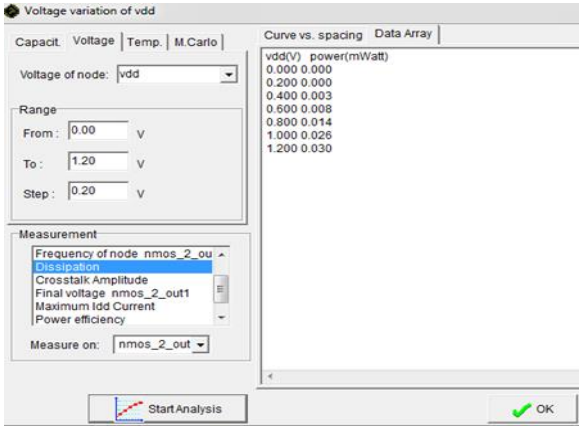

Figure 13. Leakage power dissipation for Lower Adaptive Voltage Level Circuit with Domino Inverter as Load

Power consumption is 30.156µW .. The average drain current is 0.0251 mW. Propagation delay is 1000 ps. Power dissipation is 0.030mW. Voltage at node between load & control circuit is shifted to 0.463 from 0 i.e voltage of source increases so depletion region at source bulk increases , this increases the threshold voltage & hence reduction in leakage current. Currents Idss & Iss is shown in simulation output

5. SIMULATION RESULTS

Parameters	Power Consumption (µW)	Power Dissipation (mW)	Iddavg (mA)	Voltage at node between load & loadVs (V)	Delay (ps)
INVERTER	39.254	0.039	0.033	Vss	900

LAVL with static CMOS inverter	38.160	0.038	0.032	0.722	1000
DOMINO INVERTER	34.513	0.035	0.029	Vss	1050
LAVL with Domino inverter	30.156	0.030	0.025	0.463	1000

6. CONCLUSION

Lower Adaptive Voltage Level Circuit which reduces leakage power problem was developed.This circuit increases the threshold voltage which in connection reduces leakage power .So it can be used in low leakage power applications.It also has reduced power consumption & dissipation.

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